

09/937611

September 27, 2001

**BOX PCT**

Honorable Commissioner of  
Patents and Trademarks  
Washington, D.C. 20231

Attorney Docket No 2241/50458

Re: Transmittal Letter to the United States  
Designated/Elected Office (DO/EO/US)  
Concerning a Filing Under 35 U.S.C. §371

International Application No.: PCT/JP00/02097  
International Filing Date: 31 March 2000

Priority date claimed: 31 March 1999  
Priority application number: 94369/1999

Inventorship: Michitaka FUKUDA

Title: METHOD FOR SYNCHRONOUS SERIAL  
COMMUNICATION AND SYSTEM FOR SYNCHRONOUS SERIAL COMMUNICATION

Enclosed herewith for entering the national stage in the  
United States is the above-referenced international  
application.

APPLICANT WISHES THAT THE ANNEXES TO THE INTERNATIONAL  
PRELIMINARY EXAMINATION REPORT REPLACE THE APPROPRIATE PAGES  
OF THE CLAIMS AS FILED.

1. ☒ This is a FIRST submission of items concerning a  
filing under 35 U.S.C. §371.
2. ☐ This is a SECOND or SUBSEQUENT submission  
of items concerning a filing under 35 U.S.C. §371.
3. ☒ This express request to begin national examination  
procedures (35 U.S.C. §371(f)) at any time rather  
than delay examination until the expiration of the  
applicable time limit set in 35 U.S.C. §371(b) and  
PCT Articles 22 and 39(1).

0937611 010000

4. [X] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. [X] A copy of the International Application as filed (35 U.S.C. §371(c)(2))
- a. \_\_\_\_\_ is transmitted herewith (required only if not transmitted by the International Bureau).
- b. X has been transmitted by the International Bureau (A copy of Form PCT/IB/308 is enclosed).
- c. \_\_\_\_\_ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. [X] A translation of the International Application into English (35 U.S.C. §371(c)(2)).
7. [ ] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. §371(c)(3))
- a. \_\_\_\_\_ are transmitted herewith (required only if not transmitted by the International Bureau)
- b. \_\_\_\_\_ have been transmitted by the International Bureau
- c. \_\_\_\_\_ have not been made; however, the time limit for making such amendments has NOT expired
- d. \_\_\_\_\_ have not been made and will not be made
8. [x] A translation of the amendments to the claims under PCT Article 34.
9. [ ] An oath or declaration of the inventor(s) (35 U.S.C. §371(c)(4)) is:
- [ ] Attached in the regular manner.  
[X] NOT included, but deferred under P.L. 97-247.

09/937611-0108010

09/937611

INTERNATIONAL APPLN. NO.: PCT/JP00/02097  
ATTORNEY DOCKET NO.: 2241/50458

JCO9 Rec'd PCT/PTO 27 SEP 2001

10. [ ] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5))
11. [X] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An Assignment of the invention in favor of the following organization is enclosed for recordation. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [X] A FIRST Preliminary Amendment.
- [ ] A SECOND or SUBSEQUENT Preliminary Amendment.
14. [ ] A substitute specification.
15. [ ] A change of power of attorney and/or address letter.
16. [X] Other items of information:
- [ ] Form PCT/RO/101 Request (in English/in French)
- [ ] Small Entity Declaration Under 37 C.F.R. 1.27
- [ ] Copy of Form PCT/DO/EI/905 (Notification of Missing Requirements)
- [X] 16 Sheets of Formal Drawings
- [ ] The content of the paper and computer readable copy of the attached Sequence Listing, submitted in accordance with 37 CFR §1.821(c) and (e), respectively, are the same.
- [X] Kindly appoint as associate attorneys (if not already a principal attorney) or agents:

Herbert I. Cantor, Reg. No. 24,392; James F. McKeown, Reg. No. 25,406; Donald D. Evenson, Reg. No. 26,160; Joseph D. Evans, Reg. No. 26,269; Gary R. Edwards, Reg. No. 31,824; and Jeffrey D. Sanok, Reg. No. 32,169

09/937611.01000

09/937611

JC09 Rec'd PCT/PTO 27 SEP 2001

INTERNATIONAL APPLN. NO.: PCT/JP00/02097  
ATTORNEY DOCKET NO.: 2241/50458

[X] The total amount due for the filing fee in this case  
is:

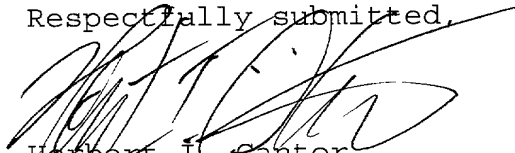
[ ] Based on Small Entity Status

Total Number of Claims: 19  
Total Independent Claims: 5

Basic filing fee, \$860/\$430. . . . .	\$ <u>860.00</u>
Independent Claims above 3, \$80/\$40 ea. . . . .	\$ <u>160.00</u>
Total claims in excess of 20, \$18/\$9 ea. . . . .	\$
Multiple dependency penalty, \$270/\$135 . . . . .	\$ <u>270.00</u>
Declaration surcharge, \$130/65 . . . . .	\$ <u>130.00</u>
English translation surcharge, \$130 . . . . .	\$
 TOTAL FILING FEE DUE . . . . .	 \$ <u>1,420.00</u>

Please forward all communications regarding this  
application to the undersigned at the letterhead address.

Respectfully submitted,

  
Herbert I. Cantor  
Reg. No. 24,392

HIC/tcv

THE COMMISSIONER IS AUTHORIZED TO CHARGE ANY FEES  
WHICH MAY BE REQUIRED OR CREDIT ANY OVERPAYMENT TO  
DEPOSIT ACCOUNT NO. 05-1323. THIS FORM IS FILED IN  
DUPLICATE.

THIS IS A GENERAL AUTHORIZATION EXCLUDING ONLY PAYMENT  
OF THE ISSUE FEE.

09/937611.010802

09/937611

JC09 Rec'd PCT/PTO 27 SEP 2001  
Attorney Docket: 2241/50458  
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: MICHITAKA FUKUDA

Serial No.: NOT YET ASSIGNED

Group Art Unit:

Filed: SEPTEMBER 27, 2001

Examiner:

Title: METHOD OF SYNCHRONOUS SERIAL COMMUNICATION AND  
SYSTEM FOR SYNCHRONOUS SERIAL COMMUNICATION

PRELIMINARY AMENDMENT

**Box NEW APPLICATION**

Commissioner for Patents  
Washington, D.C. 20231

Sir:

Please enter the following amendments to the specification, claims and  
abstract prior to the examination of the application.

IN THE CLAIMS:

Please amend Claims 3-8 (numbered as Claims 4-9) as follows:

3. (Amended) A method for synchronous serial communication as described  
in claim 1, wherein, if it is required to transmit data, mode information notifying  
under which mode the transmission of the data will be achieved is attached to the  
data to be transmitted.

4. (Amended) A method for synchronous serial communication as described in claim 1, 2, 3 or 9, wherein the serial data are divided into blocks by bytes.

5. (Amended) A system for synchronous serial communication which comprises a data transmitting component comprising:

a storage means to store data fed by an external device;

a decision means to calculate the number of clock signals required for the transmission of said data for each of the transmission modes above, and to decide which mode will allow the transmission of said data to occur in the least number of clock signals; and

an output means to choose the mode which has been decided by the decision means as allowing the transmission of said data to occur in the least number of clock signals, to read said data stored in the storage means, and to transmit said data through the communication mode thus chosen.

6. (Amended) A system for synchronous serial communication which comprises a data receiving component comprising:

a storage means to store data;

an analysis means to identify the communication mode of received data based on the received mode information; and

a control means to cause the received data to be stored in the storage means according to the mode identified by the analysis means.

7. (Amended) A method for synchronous serial communication as described in claim 1, 2, 3 or 9, wherein, if it is required to transmit a command which

concerns with the treatment of data already transmitted, firstly transmitted is command data indicating the current data carries a command concerning with the treatment of the data already transmitted, and then transmitted is said block information from which it is possible to identify the block(s) to be treated out of the data previously transmitted.

8. (Amended) A method for synchronous serial communication as described in claim 7, wherein said command includes at least either an invert command or a bit shaft command.

Please insert the following new claims:

--9. A method for synchronous serial communication as described in claim 2, wherein, if it is required to transmit data, mode information notifying under which mode the transmission of the data will be achieved is attached to the data to be transmitted.

10. A method for synchronous serial communication as described in claim 5, wherein, if it is required to transmit a command which concerns with the treatment of data already transmitted, firstly transmitted is command data indicating the current data carries a command concerning with the treatment of the data already transmitted, and then transmitted is said block information from which it is possible to identify the block(s) to be treated out of the data previously transmitted.

11. A method for synchronous serial communication as described in claim 10, wherein said command includes at least either an invert command or a bit shift command.

12. A system for synchronous serial communication which comprises a data transmitting component comprising:

a memory coupled to receive and store data fed by an external device;

a processing unit which calculates the number of clock signals required for the transmission of said data for each of the transmission modes above, and decides which mode will allow the transmission of said data to occur in the least number of clock signals; and

a selector unit, which selects a mode which has been decided by the processing unit, to read said data stored in the memory, and to transmit said data through the communication mode thus chosen.

13. A system for synchronous serial communication which comprises a data receiving component comprising:

a memory which stores data;

an analysis unit which identifies a communication mode of received data based on the received mode information; and

a control unit which causes the received data to be stored in the memory according to the mode identified by the analysis unit.

(A copy of the marked-up version of amended claim is attached to this Preliminary Amendment).



### REMARKS

Entry of the amendments to the claims before examination of the application is respectfully requested. It is noted that the Amendment Under Article 34 eliminated original claim 3 but kept all of the claims with their original numbering. In accordance with U.S. practice, the claims are re-numbered in this amendment to conform to the Rules of Practice. In addition, the claims have been amended to remove improper multiple dependencies. New claims 9 and 10 are the same as claims 3 and 7, respectively, but with different dependencies. New claims 12 and 13 are the same as claims 5 and 6, respectively, but without "means" limitations.

If there are any questions regarding this Preliminary Amendment or this application in general, a telephone call to the undersigned would be appreciated since this should expedite the prosecution of the application for all concerned.

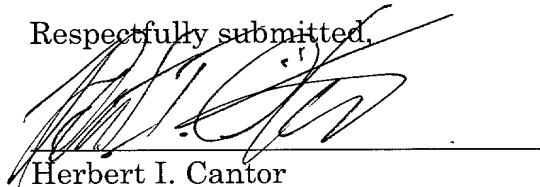
It is respectfully requested that, if necessary to effect a timely response, this paper be considered as a Petition for an Extension of Time sufficient to effect a timely response and shortages in other fees, be charged, or any overpayment in fees

093764.010803

be credited, to the Account of Crowell & Moring, LLP, Deposit Account No. 05-1323  
(Docket #2241/50458).

September 27, 2001

Respectfully submitted,



Herbert I. Cantor  
Registration No. 24,392

HIC:vca  
CROWELL & MORING, LLP  
P.O. Box 14300  
Washington, DC 20044-4300  
Telephone No.: (202) 624-2500  
Facsimile No.: (202) 628-8844

2003 SEP 27 19 26 50

**MARKED-UP VERSION SHOWING CHANGES MADE**

[4] 3 (Amended) A method for synchronous serial communication [comprising a method for synchronous serial communication] as described in claim 1 [and a method for synchronous serial communication as described in claim 2], wherein, if it is required to transmit data, mode information notifying under which mode the transmission of the data will be achieved is attached to the data to be transmitted.

[5] 4 (Amended) A method for synchronous serial communication as described in claim 1, 2, 3 or [4] 9, wherein the serial data are divided into blocks by bytes.

[6] 5 (Amended) A system for synchronous serial communication [based on the method for synchronous serial communication as described in claim 4 or 5 wherein: the] which comprises a data transmitting component comprising[.]:

a storage means to store data fed by an external device;

a decision means to calculate the number of clock signals required for the transmission of said data for each of the transmission modes above, and to decide which mode will allow the transmission of said data to occur in the least number of clock signals; and

an output means to choose the mode which has been decided by the decision means as allowing the transmission of said data to occur in the least number of

0993761.010002  
2009.11.19.2550

clock signals, to read said data stored in the storage means, and to transmit said data through the communication mode thus chosen.

[7] 6 (Amended) A system for synchronous serial communication [based on the method for synchronous serial communication as described in claim 4 or 5 wherein: the] which comprises a data receiving component comprising[.]:

a storage means to store data;

an analysis means to identify the communication mode of received data based on the received mode information; and

a control means to cause the received data to be stored in the storage means according to the mode identified by the analysis means.

[8] 7 (Amended) A method for synchronous serial communication as described in claim 1, 2, [4] 3 or [5] 9, wherein, if it is required to transmit a command which concerns with the treatment of data already transmitted, firstly transmitted is command data indicating the current data carries a command concerning with the treatment of the data already transmitted, and then transmitted is said block information from which it is possible to identify the block(s) to be treated out of the data previously transmitted.

[9] 8 (Amended) A method for synchronous serial communication as described in claim [8] 7, wherein said command includes at least either an invert command or a bit shift command.

09937641.040803  
2020101915560

16/PRTS

09/937611

JC09 Rec'd PCT/PTO 27 SEP 2001

# DESCRIPTION

## METHOD FOR SYNCHRONOUS SERIAL COMMUNICATION AND SYSTEM FOR SYNCHRONOUS SERIAL COMMUNICATION

### TECHNICAL FIELD

The present invention relates to a method for synchronous serial communication whereby it is possible to transmit serial data in synchrony with timing signals, and a system for synchronous serial communication based on the use of the method.

### BACKGROUND ART

The method for serial communication has been known as one of the methods for transmitting data serially, and many variations of the method have been devised. Serial data communication is characterized by that it requires a comparatively few communication lines, and that it allows comparatively easy data control. Because of these features, the method for serial data communication has been widely adopted by the communication systems of various fields.

However, serial data communication requires a comparatively long time if data to be transmitted are large in volume. Further, if a series of data have been dispatched, and a change must be added to the data later,

0937611-010802

usually all the data including the change must be transmitted anew. Thus, even if the change only involves a single data of the previous data, all the previous data and clock signals corresponding with those data must be transmitted anew. Because of these inconveniences, the conventional serial data communication requires a comparatively long time particularly when a data change must be added later.

Here description will be given below about the problems encountered with the conventional serial data communication, taking as an example an image forming system based on thermal ink jet printing. According to the thermal ink jet-based image forming system, a driving pulse is applied to an electro-thermal transducer element attached to an ink ejection nozzle, thereby causing a bubble to develop in ink within the ink passage leading into the nozzle; the bubble gives a sufficiently high pressure upon the ink droplet remaining close to the nozzle, to force it out as an ink jet; and the ink jet is allowed to hit against a sheet of recording paper, to print a dot there.

Such an image forming system adopts serial signal transmission in order to transmit printing data from an engine portion to a recording head portion. The engine portion or the transmitter delivers, for example, data necessary for printing a line to a memory means on the side of the receiver. For this data transmission to be properly





202011191500

pulse applied to the ink jet element according to the temperature of the element. Accordingly, the system may meet a situation where, after data necessary for printing have been delivered by the engine portion to the printing portion, the system decides to change the width of a driving pulse to be applied to a certain ink jet element in response to a detection signal from the temperature sensor of that element, and must add the change to a certain part of the data previously delivered. To put it more specifically, the system may meet a situation where, when formation of an image is started, and, during the formation, the temperature of a certain ink jet element is elevated, the system must reduce the width of a driving pulse to be applied to the ink jet element in question and add the change to the data previously sent. If the conventional image forming system meets such a situation, the system containing a memory means on the receiver side having 64 cells as described above, the system will send anew 64 clock signals, and the data to be changed in synchrony with a clock signal corresponding to a cell at which data to be changed are stored. As discussed above, according to the conventional serial data communication, even if a change must be added only to a single data out of 64 data, 64 clock signals must be sent anew together with the change, just as if all the data had to be changed. Namely, according to the conventional serial data communication, changing of the previously sent data requires an unduly

long time.

This invention was proposed with the above situation as a background, and aims at providing a method for synchronous serial communication capable of increasing the transfer speed of serial data, and a system for synchronous serial communication based on the method.

#### DISCLOSURE OF THE INVENTION

To achieve the above object, the method of this invention for synchronous serial communication comprising the step of transmitting data serially through data lines in synchrony with timing signals sent through clock line, wherein, if the transmission of a specified length of serial data is required, transmission of the data is achieved by dividing the data for transmission into a plurality of blocks, firstly transmitting block information notifying the block(s) to be transmitted, and then transmitting the data included in the block(s) notified by the block information (second mode).

The method is preferably modified so that the block information which is currently transmitted is compared with the block information which was previously transmitted, and, if the two are the same, the current block information is omitted, and the data included in the block(s) corresponding to the one(s) notified by the previous block information are transmitted (third mode).

Further, the method is preferably modified so that there are available three communication modes including, as a first mode, the conventional synchronous serial communication under which data are transmitted, not being divided into blocks; the second mode as described above; and the third mode as described above, and, if it is required to transmit data, mode information notifying under which mode the transmission of the data will be achieved is attached to the data to be transmitted.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram to indicate the outline of an image forming system based on thermal ink jet printing representing a first embodiment of this invention.

Fig. 2 illustrates how data transfer is achieved by the three modes.

Fig. 3 is a schematic diagram of a data register which stores data received by a data reception controller.

Fig. 4 is a block diagram of a data transmission controller.

Fig. 5 is a flowchart to indicate the processes achieved by a data block comparing/calculating portion.

Fig. 6 is a flowchart to indicate the processes achieved by a decision portion.

Fig. 7 is a timing chart of operations at a control portion.

Fig. 8 is a flowchart to indicate the output flow of an output circuit portion.

Fig. 9 is a timing chart of a data transmission controller.

Fig. 10 is a block diagram of a data reception controller.

Fig. 11 is a flowchart to indicate the operation of the data reception controller.

Fig. 12 is a timing chart of the data reception controller.

Fig. 13 is a block diagram of a data transfer controller representing a second embodiment.

Fig. 14 is a timing chart of signals when an invert command is transmitted.

Fig. 15 is a timing chart of signals when a bit shift command is transmitted.

Fig. 16 illustrates the flow of processes of a data reception controller representing a second embodiment

#### BEST MODE FOR CARRYING OUT THE INVENTION

(1st Embodiment)

[Constitution] A first embodiment of this invention will be described below with reference to attached figures. Fig. 1 is a schematic diagram to indicate the outline of an image forming system based on thermal ink jet printing representing a first embodiment of this invention. The

image forming system 100 based on thermal ink jet printing shown in Fig. 1 comprises an engine portion 11 including a CPU 111 and a data transmission controller 112, and a recording head portion 12 including a data reception controller 113 and a printer head 114. Data reception controller 112 is connected through a bus to CPU 111, and writes data in response to an instruction from CPU 111, or receives an instruction from CPU 111 for starting communication. Data transmission controller 112, on receipt of an instruction from CPU 111 for starting communication, determines which mode out of the communication modes described below will be most suitable for transmitting the data in a shortest possible time, adds the communication mode information informing the communication mode thus chosen to the data to be transmitted, and sends the resulting data through serial data communication to the data reception controller 113. This system communicates data between data transmission controller 112 and data reception controller 113 through synchronous serial communication. The data to be transmitted s111 are delivered through a data line in synchrony with clock signals s113 delivered through a clock line.

[Communication mode] The serial data communication responsible for the communication of data between the data transmission controller and the data reception controller of this embodiment includes three modes called a full mode,

block mode and burst mode. The full mode defines the ordinary synchronous serial communication in which data are transmitted in synchrony with serial signals. The block mode defines the communication in which, if the transmission of a specified length of serial data is required, the data to be transmitted are divided into a plurality of blocks, and first block information is sent to indicate the blocks to be transmitted, and then the data included in the blocks indicated by the block information, to achieve thereby data communication. The burst mode defines the communication in which the system compares the block information of current transmission with the block information of previous transmission, and, when it finds the two are the same, the systems omits the block information, and will transmit the data included in the blocks to be transmitted. Data transmission controller attaches to the data sent from CPU, the mode information for indicating by what mode the data will be delivered, and sends the data to data reception controller.

Fig. 2 illustrates how data transfer is achieved by the three modes. Fig. 2(a) shows the signal pattern when data transmission is achieved through the full mode; Fig. 2(b) the signal pattern when data transmission is achieved through the block mode; and Fig. 2(c) the signal pattern when data transmission is achieved through the burst mode. In the figures, SD represents data to be transmitted while SC clock signals. A bit introduced at the left end of

clock signals represents a start bit. The reason for the introduction of a start bit is to protect the system against failed operations in the presence of noises. If a start bit is transmitted, when the start bit is at high level, transmission of the data will start. The second and third bits notify mode information for setting the communication mode. If the data corresponding to the second and third bits are both zero (0), the communication mode through which the data will be transmitted will be the full mode shown in Fig. 2(a). If the data corresponding to the second and third bits are zero (0) for the former and one (1) for the latter, the communication mode responsible for data transmission will be the block mode shown in Fig. 2(b). If the data corresponding to the second and third bits are one (1) for the former and zero (0) for the latter, the communication mode for data transmission will be the burst mode shown in Fig. 2(c). Then, data transmission based on the three communication modes will be described with reference to Fig. 3. Fig. 3 is a schematic diagram of a data register which stores data received by the data reception controller. In the figure, circled figures represent addresses. Thus, the number of addresses of this data register is eight (8). Each address can contain one (1) byte of data. Accordingly, the data register shown in the figure can store  $8 \times 8$  bits, or 64 bits of data.

Let's assume now the data transmission controller will transmit data based on the full mode to the data reception

controller. Then, the data transmission controller will set data corresponding to a start bit to 1, and both of the data corresponding to 2nd and 3rd bits to 0, and then transmit the 64 data in order from the most significant bit to the least significant bit in correspondence with 64 clock signals. When the data reception controller receives a series of data as shown in Fig. 2(a), it finds, by recognizing the data corresponding to the second and third bits which are sent following a start bit are both at 0, the data will be transmitted through the full mode. Then, the same controller will store the data appearing from the fifth (5th) bit onward one after another with 8 bits as a unit into each address of the data register as shown in Fig. 3. Accordingly, if data transmission occurs on the full mode, 68 bits or 34 clock signals will be required for the data transmission.

Let's assume now the data transmission controller will transmit data based on the block mode. Then, the controller will set data corresponding to a start bit to 1, and the data corresponding to 2nd and 3rd bits to 0 and 1, then set the block information for indicating the blocks to be transmitted from the highest block to the lowest block in order. The controller will send the data included in the blocks which are set by the block information, one after another with 8 bits in order from high-order bit. With regard to the example shown in Fig. 2(b), the data are set at 1 to the 9th and 12th bits in terms of clock signals.



This indicate changes are introduced in the 3rd block (data corresponding to 31st to 24th bit) and in the 0th block (data corresponding to 7th to 0th bit). In Fig. 2(b), a change is introduced as a 0Fhex (hexadecimal data). When the data reception controller receives a series of data as shown in Fig. 2(c), it predicts, by recognizing the data corresponding to the second and third bits which are sent following a start bit are 0 and 1, the data will be transmitted through the block mode. Then, the same controller recognizes the data continuing from 5th to 12th bits in terms of clock signals carry the information about the blocks transmitted. If data transmission based on the block mode occurs as shown in Fig. 2(b), it indicates changes are introduced in the blocks 3 and 0, but the other blocks remain unchanged. When data transmission occurs based on the block mode, changed data will be delivered one after another with 8 bit from 13rd bit onward in terms of clock signals. In the particular example shown in Fig. 2(b), two blocks of data amounting to 16 bits in total are delivered. Accordingly, when the two blocks of data are delivered through the block mode as shown in Fig. 2(b), the data will require, for their delivery, 28 bits or 14 clock signals. If the same amount of data were delivered through the full mode, it would require 34 clock signals as was indicated with reference to Fig. 2(a). Therefore, data transmission based on the block mode could save a time corresponding to 20 clock signals, as compared with data

transmission based on the full mode. In other words, as long as argument is limited to the particular example as depicted in Figs. 2(a) and 2(b), transmitting data through the block mode will shorten the transmission time by a time corresponding to 20 clock signals, as compared with the conventional data transmission based on the full mode.

Let's assume now the data transmission controller will transmit data based on the burst mode. Then, the controller will set data corresponding to a start bit to 1, and the data corresponding to 2nd and 3rd bits to 1 and 0. Then, the controller will transmit the data included in the blocks changed in a descending order from the 5th bit onward one after another with 8 bits. With regard to the particular example shown in Fig. 2(c), out of the data previously sent, only the 6th block of data (data corresponding to 55th to 48th bit) is currently changed into a 0Fhex data. When the data reception controller receives a series of data as shown in Fig. 2(c), it predicts, by recognizing the data corresponding to the second and third bits which are sent following a start bit are 1 and 0, the data will be transmitted through the burst mode. Then, the same controller will write the data transmitted from 5th bit onward one after another with 8 bit over the corresponding blocks previously delivered. With regard to the particular example shown in Fig. 2(c), the data reception controller receives an 8 bit of data which will replace the 6th block of data previously

delivered. In this case, data transmission completes in a time corresponding to 6 clock signals in total.

Accordingly, replacing the previous blocks using the burst mode will save a time corresponding to 28 clock signals as compared with the case where the same purpose would be achieved by the conventional full mode, or in other words, transmitting data through the burst mode will shorten the transmission time by a time corresponding to 28 clock signals, as compared with the conventional data transmission based on the full mode.

[Constitution of data transmission controller] Next, the data transmission controller will be described with reference to Fig. 4. Fig. 4 is a block diagram of the data transmission controller. The data transmission controller comprises an address decoding portion 121 which decodes address data sent by a CPU, and determines the locations into which the data received should be written; a data register 122 which temporarily stores the data sent by the CPU in the locations nominated by the address decoding portion 121; a memory 124 for current blocks which stores currently changed blocks of data; a memory 125 for previous blocks which stores previously changed blocks of data; a block comparing/calculating portion 126 which checks by comparison whether or not the current block information are the same with the previous ones, and, if transmission of a data is required, calculates the number of clock signals required for the transmission of the data for each of the

three communication modes; a decision portion 127 which decides the communication mode most suitable for the transmission of the data, based on the comparison/calculation results from the block comparing/calculating portion 126; an output circuit portion 128 which transmits the data stored in the data register portion 122 through the mode recommended by the decision portion 127; and a control portion 123 which controls the operations of the memory for current block, memory for previous block, block comparing/calculating portion, output circuit portion, etc.

[Operation of data transmission controller] CPU 111 creates a chip select signal s121, write signal s123, addresses b122 and data 125 based on the data sent from external personal computers or the like and sends them to the data transmission controller 112. In the data transmission controller, the address decoding portion 121 analyzes addresses sent from CPU, and dispatches enable signals s124 according to which the locations of data register portion 122 to which data should be written are determined. The enable signal is a 8 bit bus, and makes it possible to replace the data assigned to a certain address of the data register with a new data, by changing the bit corresponding to that address to 1, thereby nominating the address at which replacement should occur. The address decoding portion 121 obtains the information s127 notifying which block of data have been currently updated, based on the

addresses b123 sent from CPU, and sends the information s127 to the memory for current blocks. In addition, address decoding portion 122, on receipt of a signal for starting data transmission from CPU, sends a start trigger signal s126 to the control portion 123. Control portion 123, on receipt of the start trigger signal s126, creates an instruction signal 130 and sends the signal to the block comparing/calculating portion to urge it to compare the block information s128 about the blocks currently written which is stored in the memory for current blocks with the corresponding information s129 about the blocks previously written which is stored in the memory for previous blocks, and to calculate the number of clock signals required for the transmission of data to be currently transmitted for each of the three communication modes. The block comparing/calculating portion, on receipt of the instruction signal s130 from the control portion, compares the current block information s128 with the previous block information s129, and, when it finds the two are coincident with each other, it will send a status signal s131 to the decision portion. And the block comparing/calculating portion calculates the number of clock signals required for transmitting those data on the burst mode and on the block mode, and sends signals s132 and s133 representing the calculation results for the two modes to the decision portion.

The decision portion 127, on receipt of a status

signal s131 informing the blocks to be currently transmitted coincide with the blocks previously transmitted, determines whether the current data transmission should be made on the mode giving the less calculation result out of values of signals s132 and s133 (or whether the current data transmission should occur on the block mode or on the burst mode), or whether all the data should be transmitted on the full mode to replace all the data stored in the data register 122. On the contrary, when the decision portion does not receive a status signal s131, that is, when it finds the blocks to be transmitted currently do not coincide with those previously transmitted, the portion in question determines whether the current data to replace the previous data should be transmitted on the block mode or on the burst mode. The decision made by the decision portion is transmitted as a mode information s134 to output circuit portion 128.

Output circuit portion 128, based on the mode information s134, the block information s128 about the currently fed blocks, and the register value s135 of data register 122, creates serial data s137 formatted according to the mode information, and transmits the serial data s137 and the clock signals s138 to the data reception controller in response to an output circuit trigger s136 sent from control portion 123. Output circuit portion 128, on having transmitted those data, quickly informs control portion 123 of the completion of output transmission by sending an

output completion signal s139 to the latter. Control portion 123, on receipt of the output completion signal s139, with an intention to transfer the block information s128 for the memory 124 for current blocks to the memory 125 for the previous blocks, creates a write enable signal s140 and transmits it to the memory for previous blocks. Then, the same portion creates a signal s142 for clearing the values attached to the memory 124 for the current blocks, and sends it to memory 124. So much for the description of a series of operations performed by the data transmission controller.

[Operation of block comparing/calculating portion] Fig. 5 is a flowchart to indicate the processes achieved by a data block comparing/calculating portion. At step 10, the block comparing/calculating portion 126 checks whether or not it has received an instruction signal s130 from control portion 126 which urges portion 126 to make a comparison/calculation, and when the same portion finds it has received the instruction signal 130 in question, it proceeds to step 11. Here, the block comparing/calculating portion 126 compares block information s128 of the current blocks with block information s129 of the previous blocks. When the portion 126 finds the two are the same, it proceeds to step 12 and makes a calculation consisting of multiplying the number of blocks by 4 and adding 2 (the number of clock signals required for the start bit and the setting of the mode) to the answer, and obtains the number

of clock signals required for transmitting the data on the burst mode. At step 13, the portion 126 hoists a flag s131 signifying the current data may be transmitted on the burst mode. On the other hand, if the block comparing/calculating portion 126 finds the block information s128 of current data does not coincide with the block information s129 of previous data, it proceeds to step 14, and makes a calculation consisting of multiplying the number of blocks by 4 and adding 2 (the number of clock signals required for the start bit and the setting of the mode) to the answer, and of further adding the number of clock signals required for the setting of block information, to the previous answer, to obtain thereby the number of clock signals required for transmitting the current data on the block mode. In this way, the portion 126 calculates the number of clock signals required for transmitting the current data for each one of the communication modes. However, if the current data must be sent through the full mode, the number of clock signals required for the transmission will be 34, and thus no additional calculation will be necessary, as long as the same number of data are transmitted through this mode.

[Operation of decision portion] Fig. 6 is a flowchart to indicate the processes achieved by a decision portion 127. At step 20, the portion in question checks whether or not there is hoisted at block comparing/calculating portion 126 a flag s131 signifying the two blocks coincide with each



other, and when it finds the flag is hoisted, it proceeds to step 21. At step 21, the decision portion 127 determines whether the current data transmission should be made on the mode giving the less calculation result out of values of signals s132 and s133 (or whether the current data transmission should occur on the block mode or on the burst mode), or whether all the current data should be transmitted on the full mode to replace all the previous data stored in the data register 122. On the contrary, when the decision portion finds the flag in question is not hoisted, it proceeds to step 22. At step 22, decision portion 127 compares the number of clocks signals required for transmitting the data on the block mode obtained by the block comparing/calculating portion 126 and informed through signal s133, with the corresponding number required for transmitting the same data on the full mode. If decision portion 127 finds, as a result of comparison, transmission of the data on the full mode will require less clock signals, at step 24, the portion 127 delivers a signal s134 ("00") signifying the data will be transmitted on the full mode, to the output circuit portion. On the contrary, if decision portion 127 finds transmission of the data on the block mode will require less clock signals, the portion proceeds to step 23, and delivers a signal s134 ("01") signifying the data will be transmitted on the block mode, to the output circuit portion.

[Operation of control portion] Fig. 7 is a timing chart of

operations at the control portion 123. Control portion 123, on receipt of a start trigger signal s126 dispatched by the address decoding portion 121, firstly delivers an instruction signal s130 to the block comparing/calculating portion to instruct it to make a comparison/calculation. Then, the portion 123 delivers an output trigger signal s136 to the output circuit portion to urge the latter to deliver output. Later, the control portion 123, on receipt of an output completion signal s139 signifying the completion of output delivery from the output circuit portion, creates an enable signal s140 in order to transfer the block information stored in the memory for current blocks to the memory for previous blocks, and transmits it to the memory for previous blocks. Then, the same portion 123 creates a signal s142 for clearing the data stored in the memory for current blocks, and sends it to the memory. [Operation of output circuit portion] Fig. 8 is a flowchart to indicate the output flow of the output circuit portion 128. When output circuit portion 128 finds, at step 30, it has received an output trigger s136 from the control portion, it decodes a mode information s134 dispatched by the decision portion to identify the mode for data transmission, and delivers data according to the mode thus identified. Specifically, at step 31, output circuit portion 128 checks whether or not the mode information s134 is "00". When it finds the information in question is "00", it proceeds to step 32, and fetches data stored in the data

register portion 122, and delivers those data to the data reception controller on the full mode as indicated in Fig. 2(a). Alternatively, when it finds at step 31 the mode information s134 is not "00", it proceeds to step 33, and checks whether or not the information s134 is "01". When it finds the answer is affirmative, it proceeds to step 34, and delivers relevant data to the data reception controller on the block mode as indicated in Fig. 2(b). Alternatively, when output circuit portion 128 finds at step 33 the mode information s134 is not "01", it proceeds to step 35, and delivers relevant data to the data reception controller on the burst mode as indicated in Fig. 2(c).

[Timing chart of data transmitting elements] Fig. 9 is a timing chart of the data transmission controller. In Fig. 9, an F0hex is written into the block 2 through the burst mode. CPU sends a chip select signal s121 and a write signal s123 to the address decoding portion, as well as an address signal s122 signifying the location 2 to be addressed simultaneously. Data s125 based on F0hex are written in the data register portion. The signal s135 of Fig. 9 signifies data based on F0hex are stored in the block 2 of data register portion. The address decoding portion writes the information about the block in which data has been currently replaced, into the memory for current blocks. In response to this action, a signal s128 to be dispatched from the memory for current blocks is modified such that the signal s128 for the address 2 is

raised to a high level to indicate the address 2 (block 2) of data register portion has undergone a replacement of data. Fig. 9 represents a case where data transmission occurs on the burst mode, and thus, a signal s129 to be dispatched from the memory for previous blocks is also raised to a high level at address 2, in a similar manner to the signal s128. Moreover, because data are transmitted on the burst mode in this case, a signal s131 signifying the current block information is the same with the previous block information is also kept at a high level. Next, CPU sends an address signal s122 notifying address 8 to the address decoding portion and writes data s125 based on 00hex in it. The signal notifying address 8 relates to command data, and not to data to be transferred. The address decoding portion, if it finds data are present at address 8, interprets it as representing CPU dispatches a data transmission start command. The data s125 contains 00hex, but this data do not have any specific meaning. The address decoding portion, on receipt of the data transmission start command, creates a start trigger signal s126, and delivers it to the control portion. The control portion, on receipt of the start trigger signal s126, firstly sends a comparison/calculation trigger signal s130 to the block comparing/calculating portion. Then, the control portion delivers an output trigger signal s136 to the output circuit portion. The block comparing/calculating portion, on receipt of the

comparison/calculation trigger signal s130, compares signal s129 with signal s128, and, if it finds the two signals coincide with each other, hoists a flag s131 signifying coincidence, and then calculates the number of data required for transmitting the data on the burst mode or on the block mode, and creates signals s132 and s133 based on the former and latter calculation results respectively. In this particular example, data will be transmitted on the burst mode, and thus, the signal s132 of Fig. 9 represents 6 (6D) based on decimal notation. The decision portion 127, based on the information conveyed by signals s131, s132 and s133 (not illustrated), delivers a mode information s134. In this particular case, as data will be transmitted on the burst mode, the mode information s134 of Fig. 9 represents "10" on binary notation. Output circuit portion 127, on receipt of an output trigger s136 from control portion 123, reads the data s135 stored in the data register portion, and transmits data s137 to be transmitted and clock signals s138 according to the mode information s134. Of a series of clock signals associated with the data, the first 2 clock signals concern with the information of the initial setting; the succeeding 4 clock signals relate to the transmission of data corresponding to the block 2 (data corresponding to 23rd to 16th bit) in this particular example. When transmission of data is completed, the output circuit portion informs the control portion 123 of the completion of data transmission by sending an output

completion signal s139. The control portion, on receipt of the signal s139, creates a write enable signal s140 with an intention to transfer the block information stored in the memory 124 for current blocks to the memory 125 for the previous blocks, and transmits it to the memory 125 for previous blocks. Then, the same portion creates a signal s142 for clearing the values stored in the memory 124 for the current blocks, and sends it to memory 124. So much of the description of a serial of transmitting operations performed.

[Constitution of data reception controller] Fig. 10 is a block diagram of the data reception controller. The data reception controller comprises a decoding portion 150 to decode the information carried by data s137 and clock signals s138 received, a block memory 151 to store the block information received, a data register portion 153 to store the data received, and a data register control portion 152 to deliver an enable signal which signifies that the data received are assigned to which locations of the data register portion 153, based on the mode information s152, block information s151 and clock signals s138.

[Operation of data reception controller] Fig. 11 is a flowchart to indicate the operation of the data reception controller. At step 40, when decoding portion 150 detects the data of a start bit is "1", data reception becomes ready. At step 41, the data reception controller checks

whether or not the data of the second bit is "1", and, when it finds the data in question is "1", it proceeds to step 42. At step 42, the data reception controller handles the data received, and performs the operation of the burst mode, that is to say, stores the data one after another in the relevant block of the data register portion, by referring to the previous block information. If at step 41 the data reception controller finds the data of the second bit is not "1", it proceeds to step 43, and checks whether or not the data of the third bit is "1". If the controller finds the data in question is "1", it proceeds to step 44, and handles the data received, and performs the operation of the block mode, that is to say, stores, in the block memory, the block information notifying whether or not data for each block should be written into the memory, according to the signals subsequently transmitted. Then, the data reception controller stores the data corresponding to the relevant block in a descending order of block in the data register portion, by referring to the block information stored in the block memory. However, if at step 43 the data reception controller finds the data of the third bit is not "1", it proceeds to step 46, and handles the data received, and performs the operation of the full mode, that is to say, stores all the transmitted data in a descending order in the data register. Then, at step 47, it stores the block information notifying all the data corresponding to every block have been completely written, into the block

memory.

Fig. 12 is a timing chart of the data reception controller. This figure concerns with a case where data transmission occurs on the burst mode, and data based on F0hex is written into the block 2 on the burst mode. Because the current data transmission will occur on the burst mode, the previous block information is stored in the block memory 151, which is indicated by a signal s151 kept at a high level for the block 2. The data reception controller, based on the signal s151, can identify, for a given data received, the block of memory into which the data should be stored. The data reception controller, by referring to the data of the 2nd and 3rd bits subsequent to a start bit, finds the current transmission mode is the burst mode, sets a signal s152 to "10" which is data indicative of the burst mode, and sends the signal to the data register control portion 152. The data register control portion 152, based on the mode information s152 and the block information s151, creates an enable signal s153 which is a select signal for allocating the data transmitted in association with clock signals from the 5th bit onward, to their proper addresses, and sends the signal to the data register portion 153 so that the data from the 5th bit onward are properly stored there. The data stored in the data register portion 153 are then sent to a printer head as printing data.

(2nd Embodiment)



[Constitution] Next, the second embodiment of this invention will be described with reference to the attached drawings. Fig. 13 is a block diagram of the data transmission controller of an image forming system based on thermal ink jet printing representing a second embodiment. The data transmission controller of the second embodiment shown in Fig. 13 is different from the corresponding controller of the first embodiment shown in Fig. 4 in that, in the former, an address decoding portion creates an invert trigger s201, shift trigger s202 and side data s203, and deliver them as output. Otherwise the former is the same with the latter. Hence, the elements of the second embodiment having functions similar to those of the first embodiment will be represented by the same symbols, and their detailed description will be omitted. The elements of the second embodiment similar to those of the first embodiment will be omitted from further description. The invert trigger s201 carries an instruction for inverting data already sent to the data receiving elements. The shift trigger s202 carries an instruction for shifting data already sent to the data receiving elements by a specified number of bits. The side data s203 represent the data placed at the bit end after the data has been shifted by a specified number of bits under the influence of a shift trigger. The data transmission controller identifies the contents of signals s201, s202 and s203, by decoding addresses sent by CPU. For example, an agreement is made

such that address 9 is assigned to signal s201, address 10 to signal s202 and address 11 to signal s203.

[Operation] Let's assume the data transmission controller receives from CPU instructions to invert the data corresponding to the blocks 1 and 0 respectively. Address decoding portion 121 decodes the instructions, and causes the memory for current blocks to store the block information carrying the instruction to invert the data corresponding to the blocks 1 and 0 respectively. In addition, the address decoding portion 121 creates an invert trigger s201, and sends it to output circuit portion 128. The output circuit portion 128, on receipt of the invert trigger s201, recognizes data to be inverted must be the data corresponding to the block 1 and 0 based on a signal s128, and sends the information about the data corresponding to the blocks to be inverted as well as the invert trigger to the data receiving elements. Fig. 14 is a timing chart of signals when an invert trigger s201 is transmitted. When the address decoding portion 121 sends an invert trigger s201 to the control portion 123 and the output circuit portion 123, the control portion 123 creates an output trigger s136, and sends it to the output circuit portion 128. The output circuit portion 128, on receipt of the output trigger s136, sends information carrying the instruction to invert the data corresponding to the blocks 1 and 0 to the data receiving elements in synchrony with clock signals. Specifically, the output circuit portion

128 sets the data corresponding to a start bit to 1, and both of the data corresponding to the 2nd and 3rd bits to 1. The last bit array indicates the data to be transmitted after this concern with an instruction. The same portion 128 further sets the data of the 4th bit to 0 which indicates the instruction concerns with the inversion of data. The bit arrays from 5th to 12th bits are portions for setting the block information, and in this particular example, the data of 11th and 12th bits are set to 1.

With reference to Fig. 15, description will be given of a case where the data transmission controller receives from CPU instructions to shift the data corresponding to the block 1 by one (1) bit rightward (towards a lower position) and to set the most significant bit of the data corresponding to the block 1 being shifted, to 0. Fig. 15 is a timing chart of signals when a shift trigger s202 is transmitted. When the data transmission controller receives those instructions, the address decoding portion 121 sends a shift trigger s202 to the control portion 123 and the output circuit portion 128. The control portion 123, on receipt of the shift trigger s202, sends an output trigger s136 to the output circuit portion 128. The output circuit portion 128, on receipt of the output trigger s136, transmits, to the data receiving elements, information carrying the instruction to shift the data corresponding to the block 1 by a specified number of bits, in synchrony with clock signals. Specifically, the output circuit

portion 128 sets the data corresponding to a start bit to 1, and both of the data corresponding to the 2nd and 3rd bits to 1. The same portion 128 further sets the data of the 4th bit to 1, indicating the instruction concerns with the shift of data; the data of 5th bit to 0, indicating the shift should occur rightward; and the data of 6th bit to 0, indicating the end bit is set to 0. The bit arrays from 7th to 14th bits are portions for setting the block information, and in this particular example, the data corresponding to 13th bit is set to 1.

Fig. 16 illustrates the flow of processes of a serial controller serving as one of the data receiving elements. It is the same with the corresponding one of the first embodiment shown in Fig. 11 in steps 40 to 47, and is different only in step 51 onward. Accordingly, here steps 40 to 47 will be omitted from description, and only step 51 onward will be described. When the serial controller finds, at step 41, the data of 2nd bit is 1, it proceeds to step 51. Then, it checks whether or not the data of 3rd bit is 1. When the serial controller finds the data in question is not 1, it proceeds to step 42, and performs similar operations as in step 42 of the first embodiment. On the contrary, if the serial controller finds, at step 51, the data of 3rd bit is 1, it proceeds to step 52, and checks whether or not the data of 4th bit is 1. When the controller finds the data in question is not 1, it proceeds to step 53, and inverts the data corresponding to the

specified blocks. On the contrary, if the serial controller finds the data of 4th bit is 1, it proceeds to step 54, and checks whether or not the data of 5th bit is 1. When it finds the data in question is 1, it proceeds to step 55, and checks whether or not the data of 6th bit is 1. When the serial controller finds the data of 6th bit is not 1, it proceeds to step 56, shifts the data corresponding to the specified blocks leftward, and sets the least significant bit to 0. On the contrary, if the serial controller finds, at step 55, the data of 6th bit is 1, it proceeds to step 57, shifts the data corresponding to the specified blocks leftward, and sets the least significant bit to 1. When the controller finds, at step 54, the data of 5th bit is not 1, it proceeds to step 60, and checks whether or not the data of 6th bit is 1. If it finds the data in question is 1, it proceeds to step 61, shifts the data corresponding to the specified blocks rightward, and sets the most significant bit to 1. If it finds the data of 6th bit is not 1, it proceeds to step 62, shifts the data corresponding to the specified blocks rightward, and sets the most significant bit to 0.

As it is possible according to this embodiment to invert or shift data corresponding to any desired block sent to the data receiving elements by using an invert command and a shift command as mentioned above, and simply transmitting the invert command or the shift command together with the block information, transmitting data will

occur faster as compared with the first embodiment where transmission of data occurs in the three different communication modes.

[Advantages obtained from the embodiments] According to the embodiments described above, it is possible to automatically select, through the arrangement of hardware element, a mode out of the three communication modes available that is most appropriate for quickly transmitting given data, based on the data written by an external computer or the like, and to transmit the data. The data receiving element stores the data thus received into the register according to the content of mode information attached to the data. Through this arrangement it is possible for the data receiving element to reduce the time necessary for serial communication, without being conscious of the speed of serial communication. Further, if the system desires, of the data already sent to the data receiving element, to shift a certain bit, or to invert a certain bit, the system can achieve the object by creating a shift command or an invert command, and simply attaching the command to the block information, which will relieve the system of the necessity of preparing bit shifts or bit inverts for individual data involved as in the conventional system. This will further contribute to the contraction of the time necessary for serial communication.

[Other possible embodiments] This invention, however, is not limited to the above embodiments, and various

modifications thereof will be possible within the scope of this invention. For example, according to the above embodiments, description has been given on the assumption that a block of data has an eight (8) bit length. However, a block of data may have a length equal to 16 bits, 32bits, etc. Further, according to the above embodiments, description has been given on the assumption that this invention is embodied in an image forming system. However, this invention is not limited to such equipment. For example, this invention may be profitably utilized for common communication based on communication lines. Furthermore, according to the above embodiments, data communication may occur on the block mode, burst mode or full mode. However, data communication supported by this invention is not limited to this case: data communication based on this invention may occur on the block mode alone, on either the block mode or burst mode, or on either the block mode or full mode.

#### INDUSTRIAL APPLICABILITY

As discussed above, this invention provides a method for synchronous serial communication whereby it is possible to reduce the time required for data transmission as compared with the conventional communication method, by dividing serial data to be transmitted into a plurality of blocks, to firstly transmit a block information, and then

to transmit data corresponding to the block notified by the block information.

As the method makes the system to choose any one among the three communication modes consisting of the first, second and third modes, it is possible for the system to choose, according to data to be transmitted, the mode that allows the fastest transmission of the data.

It is possible to further reduce the time for data transmission by creating a command for treating the data already sent to the data receiving element, and a block information, then by sending them to the data receiving element, and by treating the data corresponding to the block already sent to the data receiving element.

As discussed above, the method for synchronous serial communication and the system for serial communication of this invention are applicable to the image forming system based on thermal ink jet printing, or to the common communication based on communication lines.



## CLAIMS

1. (After amendment) A method for synchronous serial communication comprising the step of transmitting data serially through data lines in synchrony with timing signals sent through clock line, wherein:

if it is required to transmit a specified length of serial data, the data receiving component is caused to store the specified length of serial data previously received; and

there are available a first mode, or the conventional synchronous serial communication under which data are transmitted without being divided into blocks, and a second mode under which data to be transmitted are divided into blocks, firstly transmitted is block information notifying the block(s) to be transmitted, and then transmitted are the data included in the block(s) notified by the block information, and, on the data for the block(s) in which data remain unchanged, the corresponding previous data stored in the data receiving component are used; and

the number of clock signals required for the data transmission based on the first mode, and the number of clock signals required for the data transmission based on the second mode are calculated, and compared, and transmission of the data is achieved through the mode that is found to give the less number of clock signals for transmission of the data.

2. (After amendment) A method for synchronous serial communication as described in claim 1 wherein the block information which is currently transmitted is compared with the block information which was previously transmitted, and, if it is found the block(s) in which data are currently changed is(are) the same with the block(s) in which data were previously changed, a third mode is chosen under which the current block information is omitted, and the data included in the block(s) corresponding to the one(s) notified by the previous block information are transmitted in succession, and, on the data for other block(s), the corresponding previous data stored in the data receiving component are used.

3. (Omitted)

4. (After amendment) A method for synchronous serial communication comprising a method for synchronous serial communication as described in claim 1 and a method for synchronous serial communication as described in claim 2, wherein, if it is required to transmit data, mode information notifying under which mode the transmission of the data will be achieved is attached to the data to be transmitted.

5. (After amendment) A method for synchronous serial communication as described in claim 1, 2 or 4 wherein the serial data are divided into blocks by bytes.

6. (After amendment) A system for synchronous serial communication based on the method for synchronous serial

communication as described in claim 4 or 5 wherein:

the data transmitting component comprising,

a storage means to store data fed by an external device;

a decision means to calculate the number of clock signals required for the transmission of said data for each of the transmission modes above, and to decide which mode will allow the transmission of said data to occur in the least number of clock signals; and

an output means to choose the mode which has been decided by the decision means as allowing the transmission of said data to occur in the least number of clock signals, to read said data stored in the storage means, and to transmit said data through the communication mode thus chosen.

7. (After amendment) A system for synchronous serial communication based on the method for synchronous serial communication as described in claim 4 or 5 wherein:

the data receiving component comprising,

a storage means to store data;

an analysis means to identify the communication mode of received data based on the received mode information; and

a control means to cause the received data to be stored in the storage means according to the mode identified by the analysis means.

8. (After amendment) A method for synchronous serial

communication as described in claim 1, 2, 4 or 5 wherein,  
if it is required to transmit a command which concerns with  
the treatment of data already transmitted, firstly  
transmitted is command data indicating the current data  
carries a command concerning with the treatment of the data  
already transmitted, and then transmitted is said block  
information from which it is possible to identify the  
block(s) to be treated out of the data previously  
transmitted.

9. A method for synchronous serial communication as  
described in claim 8 wherein said command includes at least  
either an invert command or a bit shift command.

FIG. 1

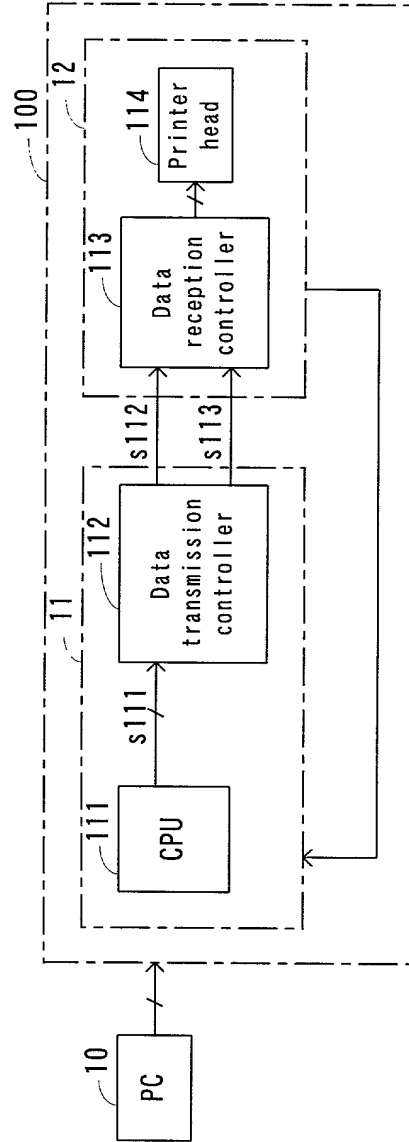


FIG. 2

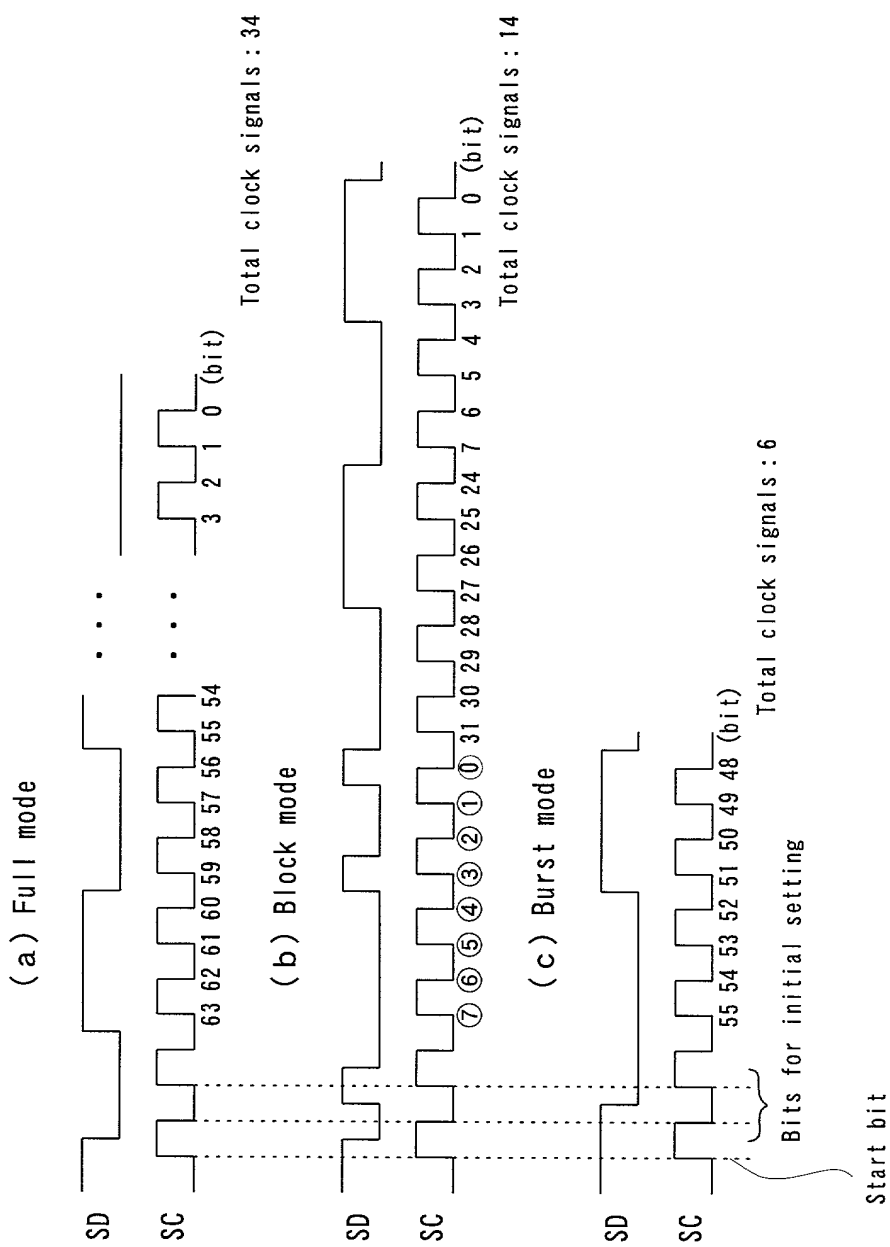


FIG. 3

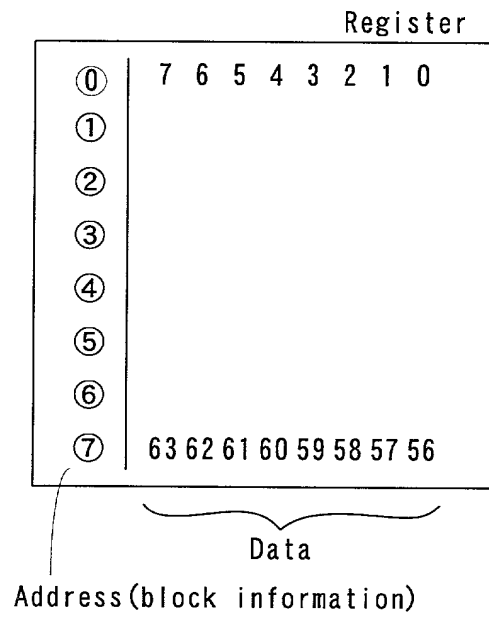


FIG. 4

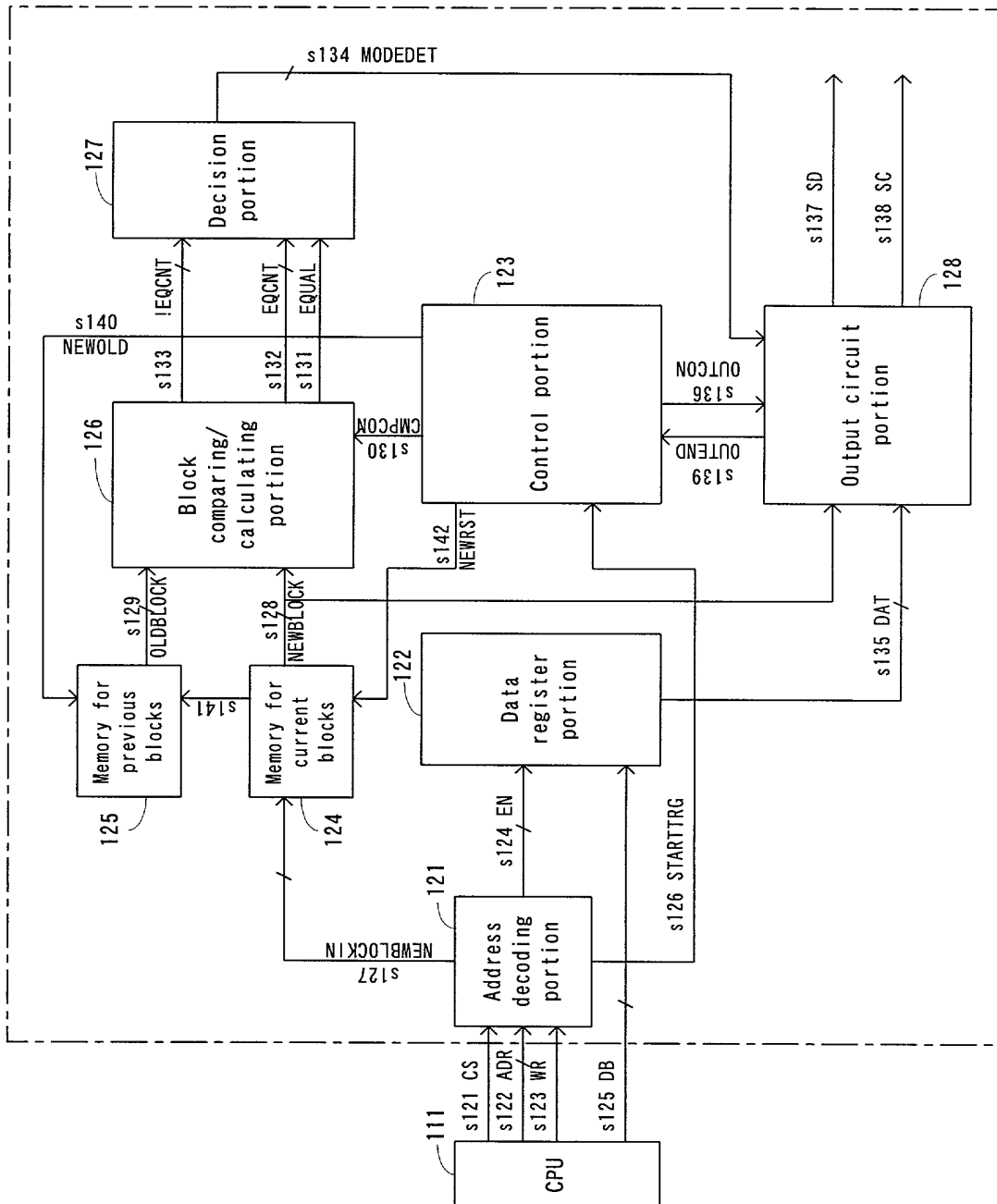




FIG. 5

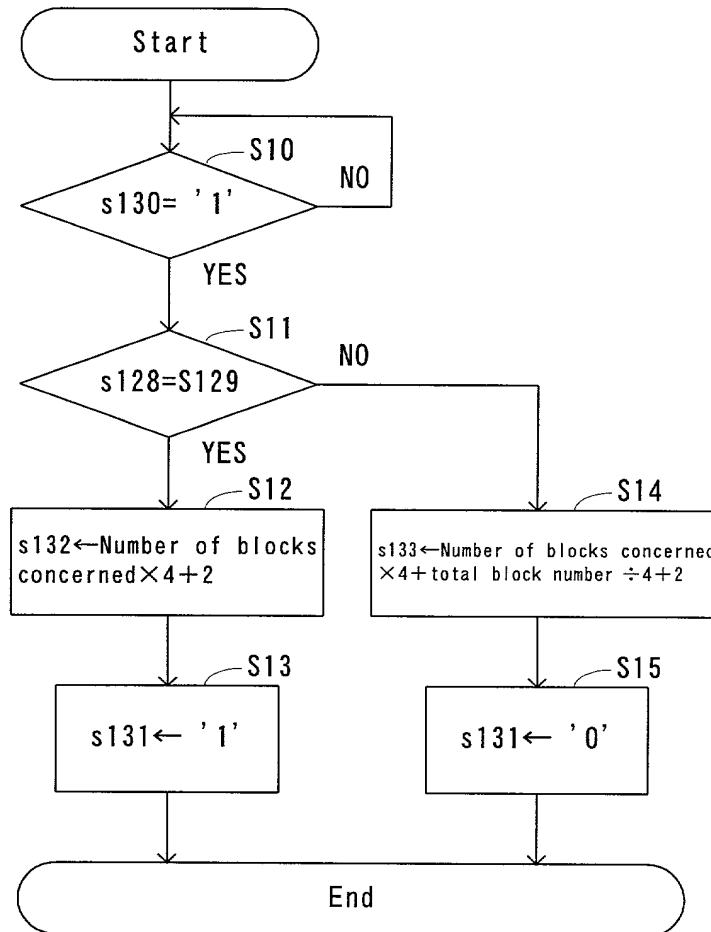


FIG. 6

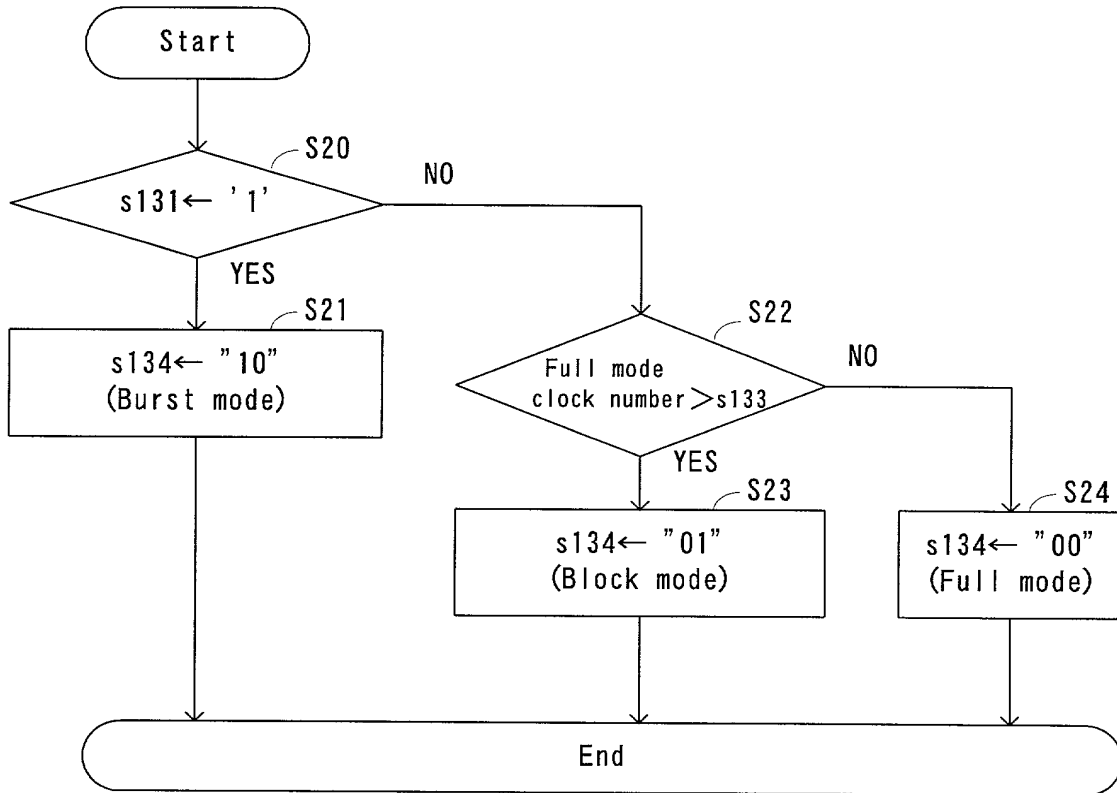


FIG. 7

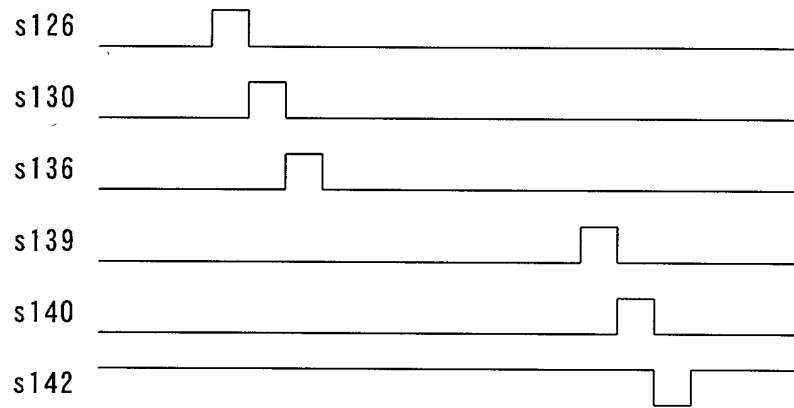


FIG. 8

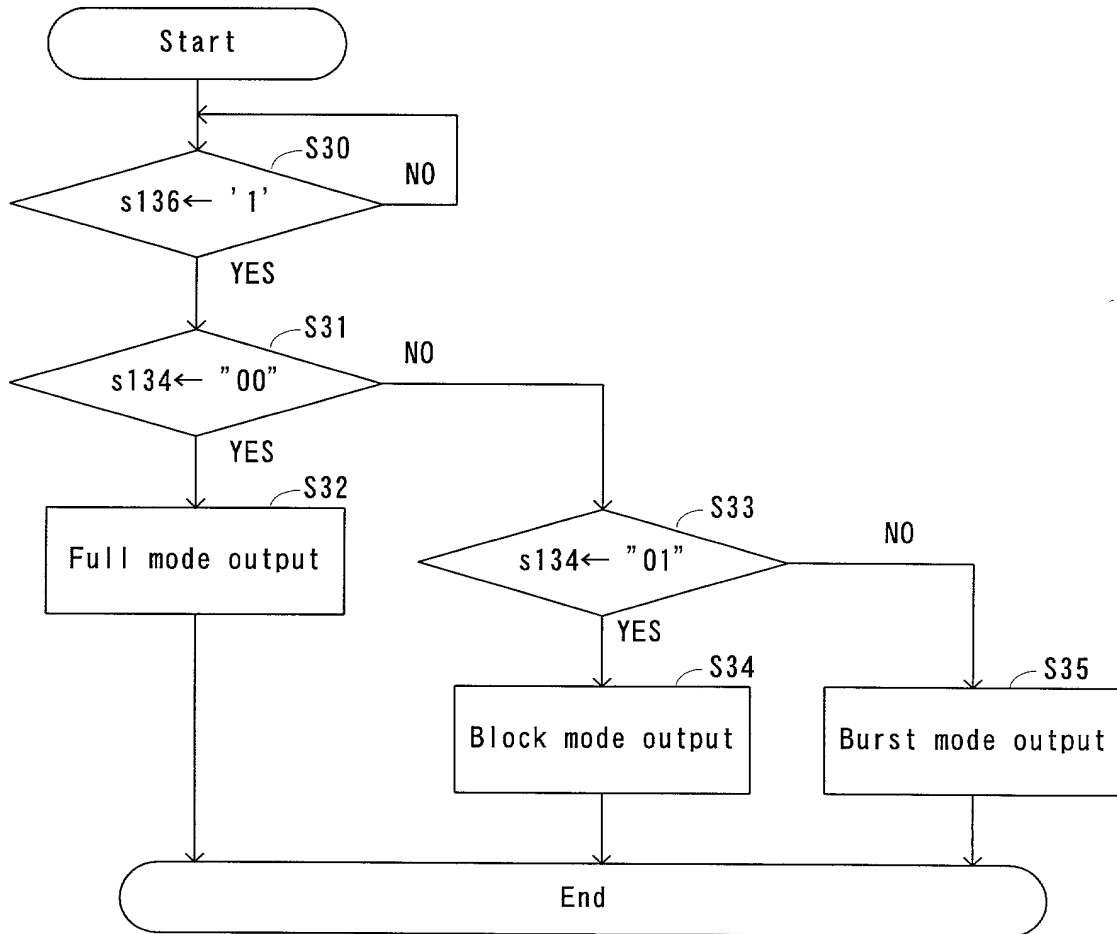


FIG. 9

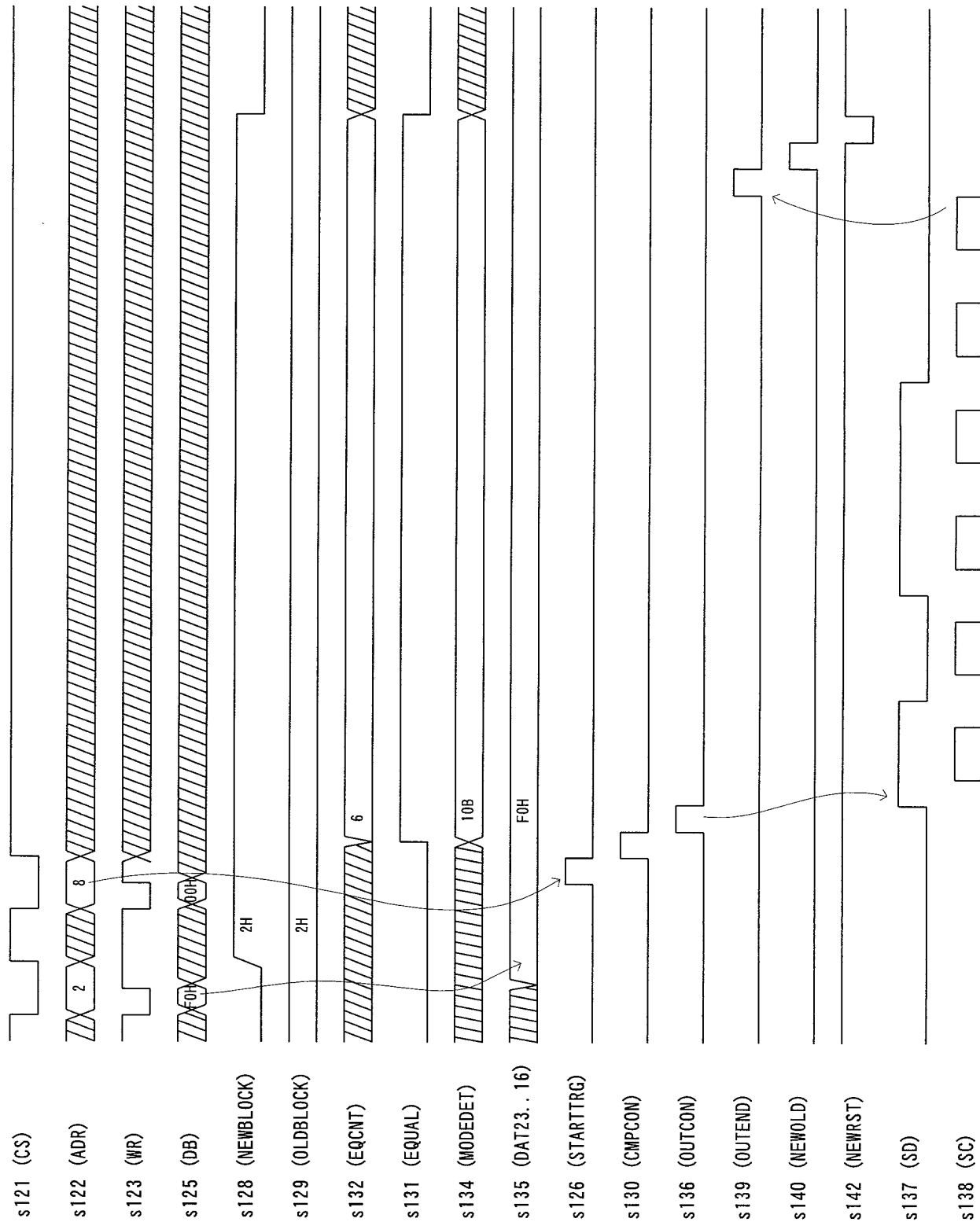


FIG. 10

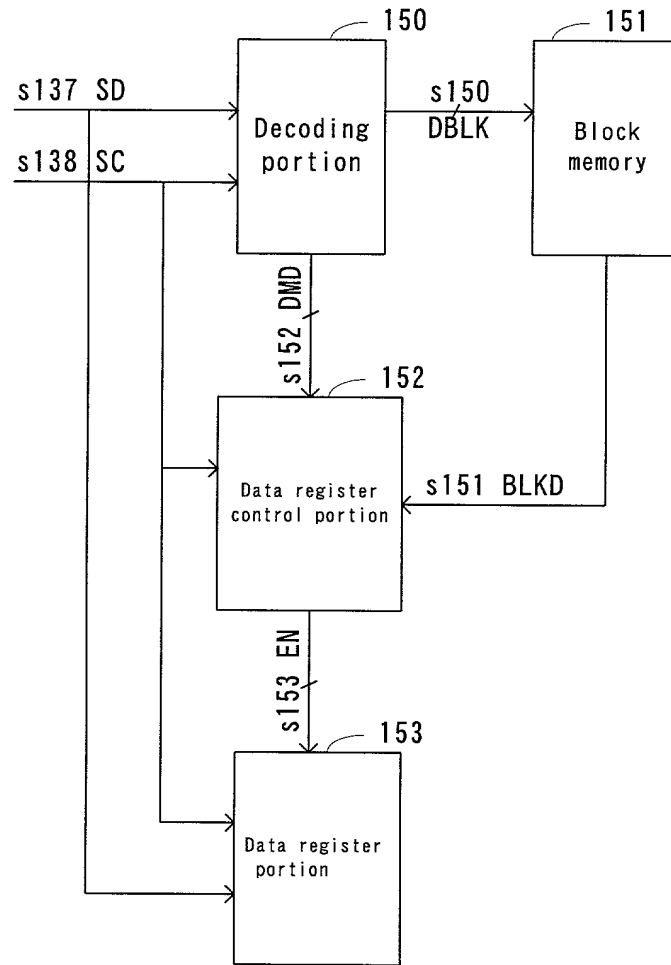


FIG. 11

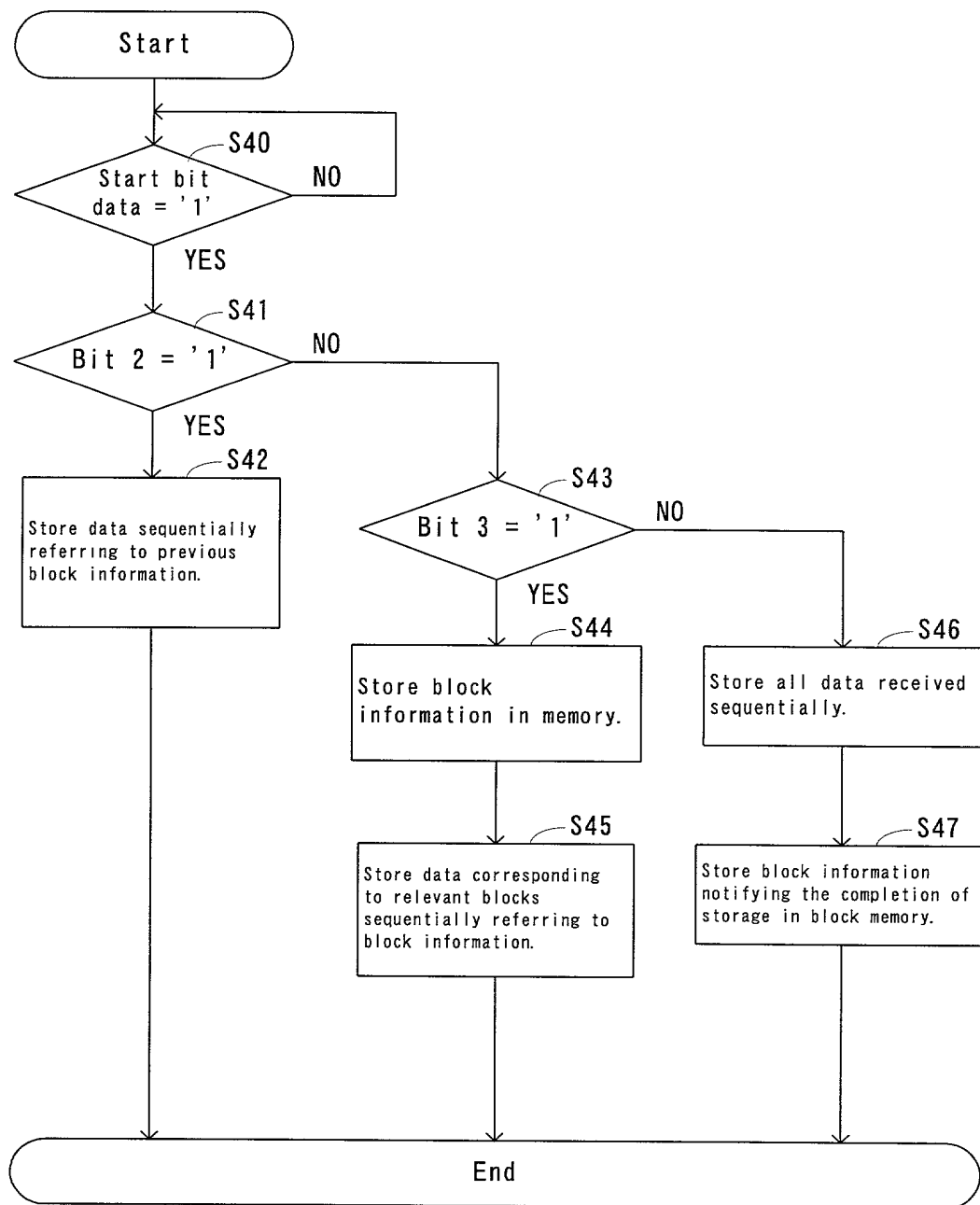
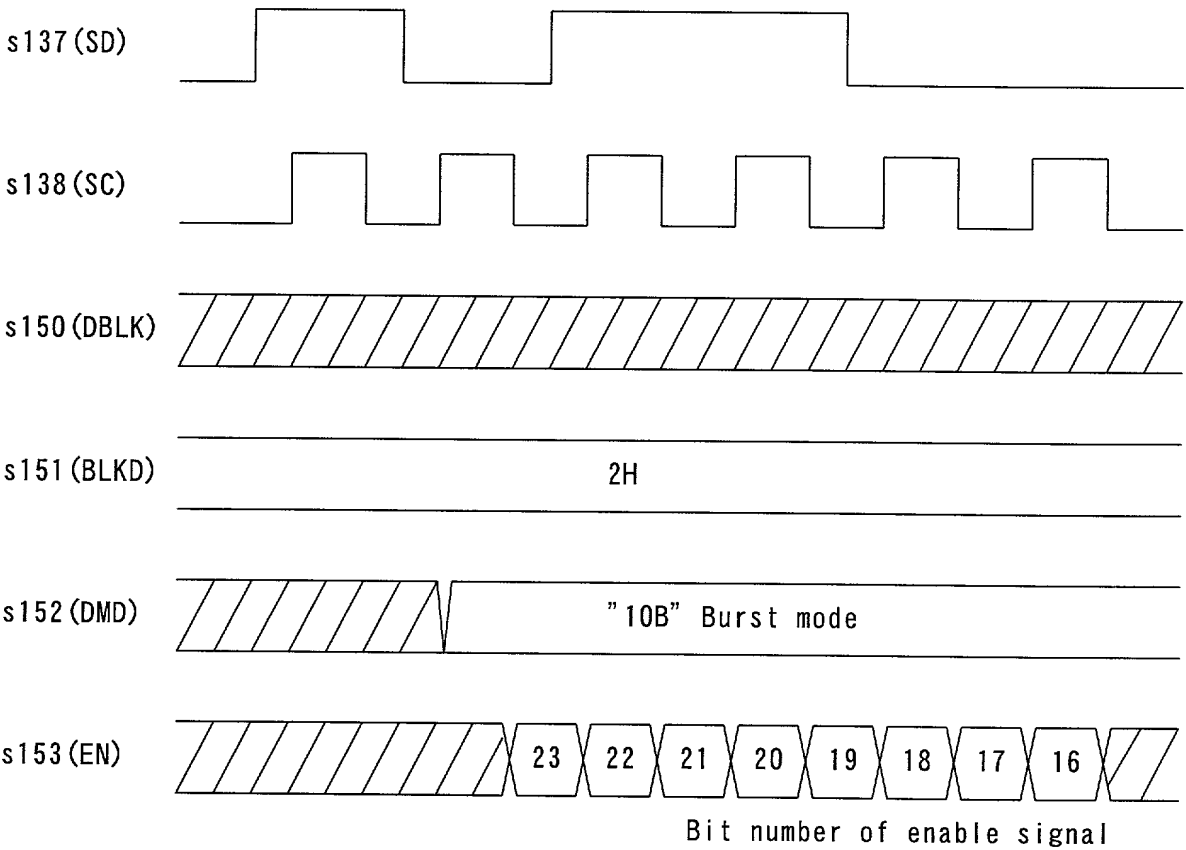


FIG. 12



20250707 19:26:00



FIG. 13

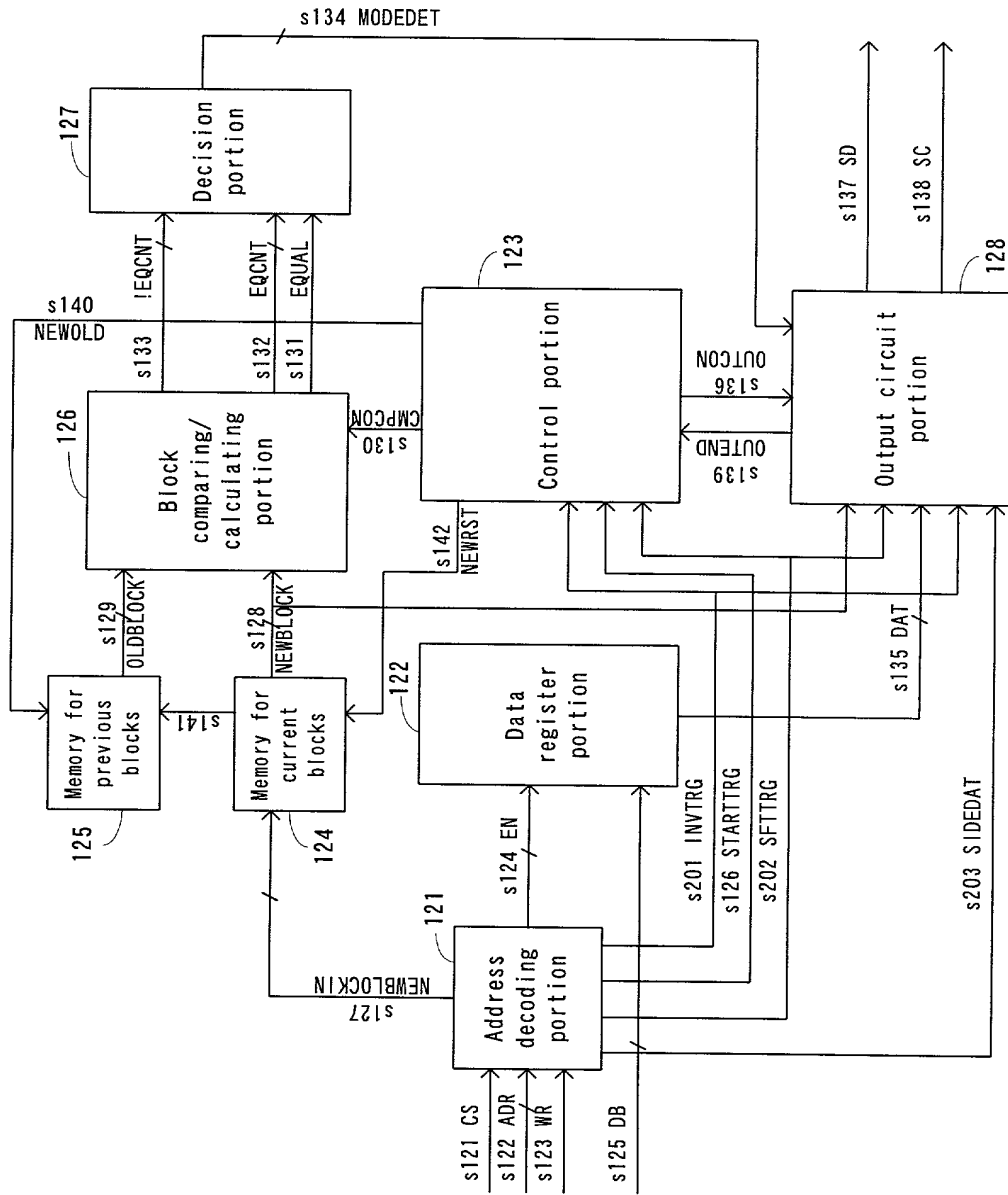


Table 1. Demographic characteristics of the study population	
Age (years)	65.0 ± 10.0
Gender	
Male	50 (50.0%)
Female	50 (50.0%)
Education (years)	12.0 ± 2.0
Marital status	
Married	40 (80.0%)
Single	10 (20.0%)
Occupation	
Retired	30 (60.0%)
Unemployed	20 (40.0%)
Income (USD/month)	1000.0 ± 500.0
Health status	
Good	40 (80.0%)
Poor	10 (20.0%)
Smoking status	
Smoker	10 (20.0%)
Non-smoker	40 (80.0%)
Alcohol consumption	
Drinker	10 (20.0%)
Non-drinker	40 (80.0%)
Comorbidities	
Hypertension	20 (40.0%)
Diabetes	10 (20.0%)
Cholesterol	15 (30.0%)
Arthritis	10 (20.0%)
Depression	5 (10.0%)
Other	5 (10.0%)

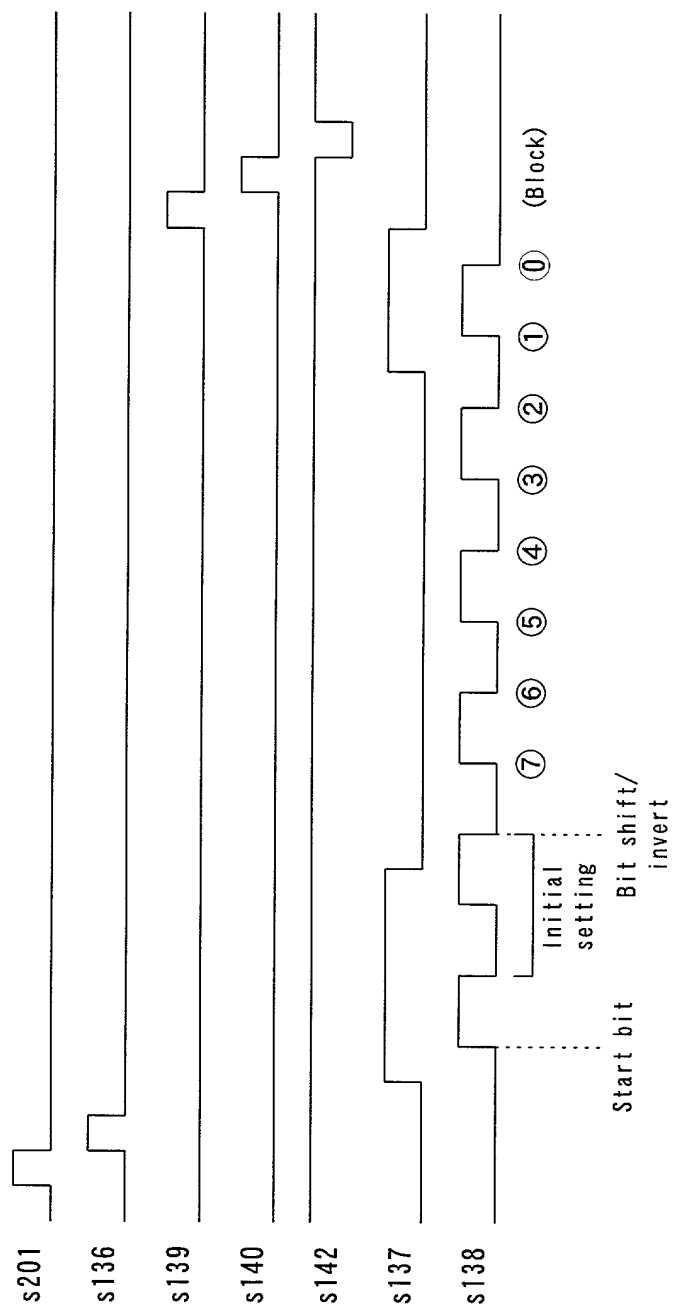
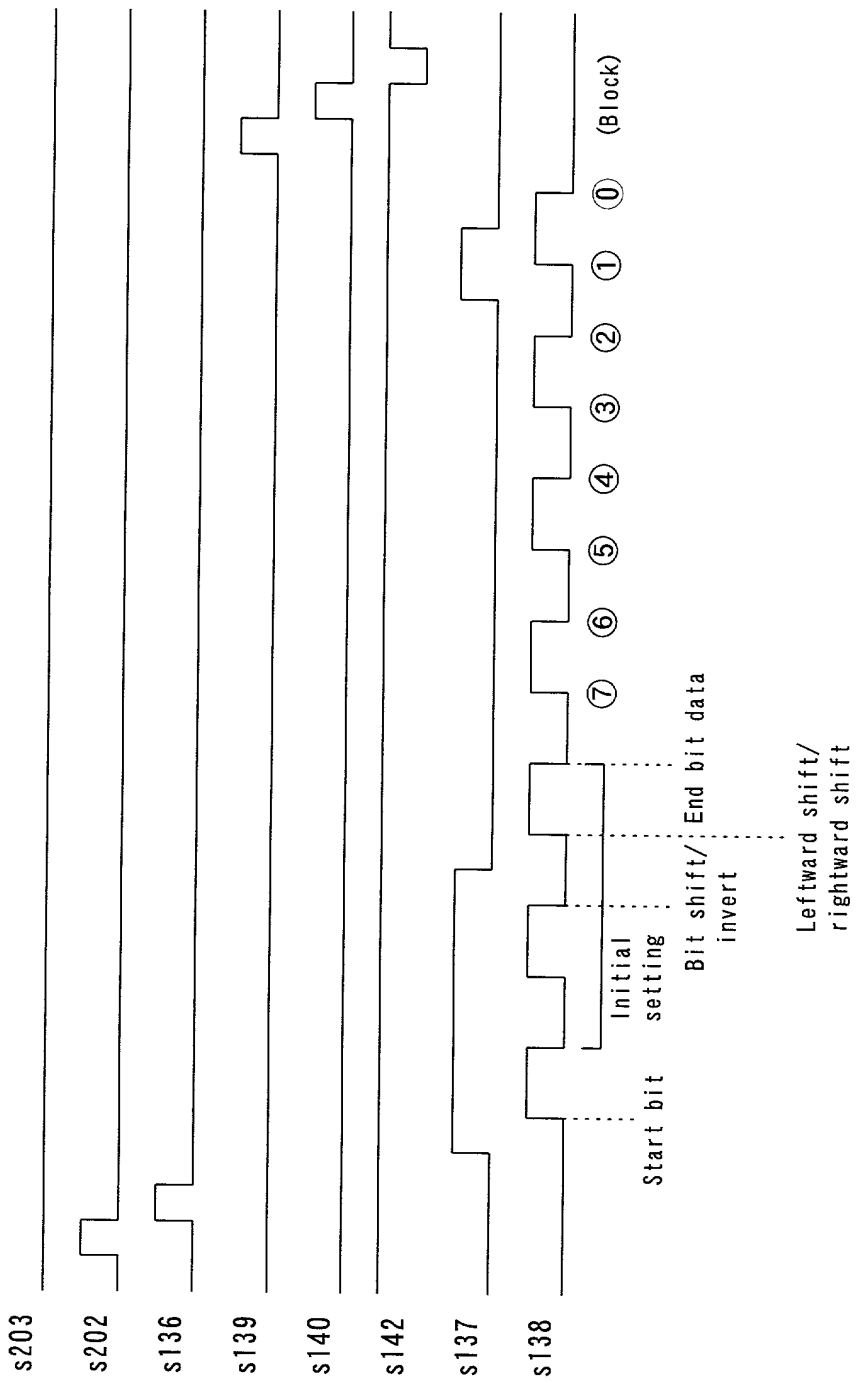


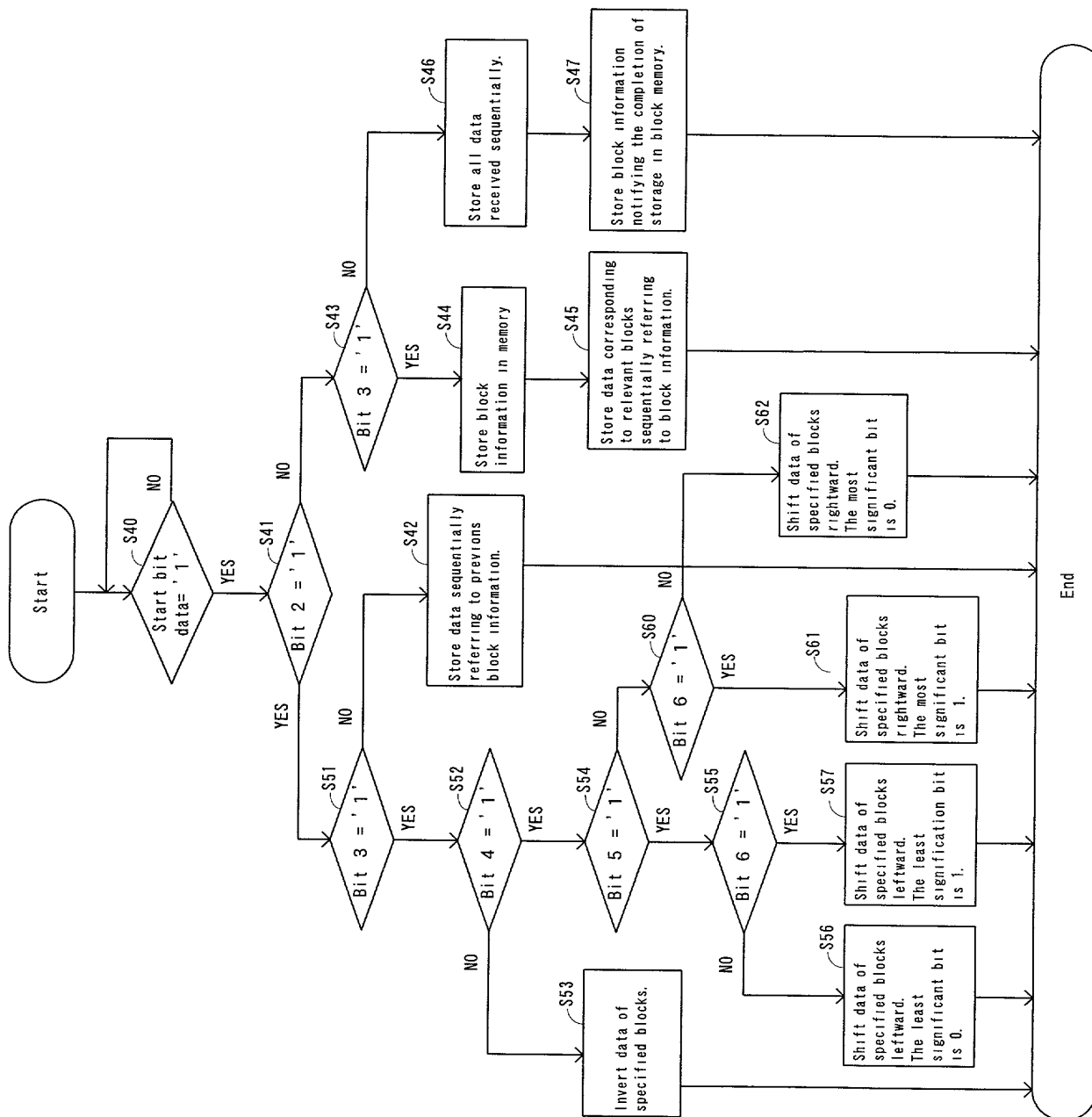
FIG. 15



09/937611

16/16

FIG. 16



UTILITY PATENT  
OR DESIGN  
SOLE OR JOINT

**CROWELL & MORING, L.L.P.**

ATTORNEY'S DOCKET NO.  
2241/50458

**UNITED STATES LETTERS PATENT  
DECLARATION AND POWER OF ATTORNEY**

As a below named inventor, I declare that I believe I am the original, first and sole inventor if only one name is listed at Item 201 below, or a joint inventor if plural names are listed below at Items 201 et. seq. of subject matter which is claimed and for which a patent is sought for the invention entitled: METHOD FOR SYNCHRONOUS SERIAL COMMUNICATION AND SYSTEM FOR SYNCHRONOUS SERIAL COMMUNICATION

which is described and claimed in:

101 ☐ the attached specification ☒ the specification in application Serial No.  
09/937,611

filed  
September 27, 2001

and (if applicable) amended on

102 ☒ International (PCT) Application No. PCT/JP00/02097

Filed: March 31, 2000

and as amended on (if any)

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known by me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim the benefit of priority, under Title 35, United States Code, §119, of any foreign application(s) for patent or inventor's certificate listed in Item 103 below and have also identified in Item 103 below any foreign application(s) for patent or inventor's certificate having a filing date before that of the application for which priority is claimed.

I hereby claim the benefit, under Title 35, United States Code, §120, of any U.S. application(s) listed in Item 105 below. If this application is a continuation-in-part, insofar as the subject matter of any of the claims thereof is not disclosed in the prior U.S. application(s) identified in Item 105 below in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior U.S. application(s) identified in Item 105 below and the national or PCT international filing date of this application.

103 FOREIGN APPLICATION(S), IF ANY, FILED WITHIN 12 (6 if a Design) MONTHS PRIOR TO THE FILING DATE OF THIS APPLICATION  
THE PRIORITY OF WHICH WHERE PERMITTED IS HEREBY CLAIMED UNDER 35 U.S.C. § 119

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED	
			YES	NO
JAPAN	11-94369	31 March 1999	X	

105 THIS APPLICATION IS A:

☐ CONTINUATION ☐ CONTINUATION-IN-PART  
☐ DIVISION ☐ OF PRIOR U.S. APPLICATION

SERIAL NO.

FILED

**POWER OF ATTORNEY:** As a named inventor, I hereby appoint the following attorney(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

JAMES F. McKEOWN  
Registration No. 25,406

HERBERT I. CANTOR  
Registration No. 24,395

DONALD D. EVENSON  
Registration No. 26,160

JOSEPH D. EVANS  
Registration No. 26,269

GARY R. EDWARDS  
Registration No. 31,824

JEFFREY D. SANOK  
Registration No. 32,169

SEND CORRESPONDENCE TO:

CROWELL & MORING, L.L.P.  
P.O. Box 14300  
Washington, D.C. 20044-4300

DIRECT TELEPHONE CALLS

202-624-2500

Inventor(s) name must include at least one unabbreviated first or middle name.

201	FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
	RESIDENCE CITIZENSHIP	CITY OR OTHER LOCATION	STATE OR COUNTRY	CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS		
202	FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
	RESIDENCE CITIZENSHIP	CITY OR OTHER LOCATION	STATE OR COUNTRY	CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS		
203	FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
	RESIDENCE CITIZENSHIP	CITY OR OTHER LOCATION	STATE OR COUNTRY	CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS		
204	FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
	RESIDENCE CITIZENSHIP	CITY OR OTHER LOCATION	STATE OR COUNTRY	CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS		
205	FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
	RESIDENCE CITIZENSHIP	CITY OR OTHER LOCATION	STATE OR COUNTRY	CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS		
206	FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME
	RESIDENCE CITIZENSHIP	CITY OR OTHER LOCATION	STATE OR COUNTRY	CITIZENSHIP
	POST OFFICE ADDRESS	POST OFFICE ADDRESS		

[ ] Seventh (and more) coinventors on page 3

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of any patent issue thereon

SIGNATURE OF INVENTOR 201	SIGNATURE OF INVENTOR 202	SIGNATURE OF INVENTOR 203
DATE	DATE	DATE
SIGNATURE OF INVENTOR 204	SIGNATURE OF INVENTOR 205	SIGNATURE OF INVENTOR 206
DATE	DATE	DATE